CLAIMS

1. An FET switch having a clamp circuit comprising:

an FET switching transistor;

a surge detector coupled between a conductive path of the FET switching transistor and a gate thereof, the surge detector having means for enabling the measurement of BVdss of the FET switching transistor;

a first biasing circuit coupled to the gate of the FET switching transistor providing a first biasing current to the gate;

a second biasing current coupled to the gate of the FET switching transistor providing a second biasing current to the gate, the second biasing current being less than the first biasing current; and

a biasing switching circuit coupled to the first biasing circuit to disconnect the flow of the first biasing current when a voltage surge is detected by the surge detector, whereby the surge detector can turn on the FET switching transistor to clamp the surge voltage below the BVdss thereof.

2. The FET switch of Claim 1 wherein the means for enabling the measurement of BVdss is a resistor in series with the surge detector.

3. The FET switch of Claim 1 wherein the FET switch is coupled to an inductive load.

4. The FET switch of Claim 3 wherein the inductive load is a solenoid in an ABS brake system.

5. The FET switch of Claim 1 wherein the surge detector comprises a zener diode.

6. The FET switch of Claim 5 wherein the surge detector comprises a plurality of zener diodes.

7. The FET switch of Claim 5 wherein the surge detector comprises a diode which prevents reverse conduction through the zener diode.

8. The FET switch of Claim 6 wherein the surge detector comprises a diode which prevents reverse conduction through the plurality of zener diodes.

9. The FET switch of Claim 1 wherein the first bias current is substantially 20 ma. and the second bias current is substantially 80 microamps.

10. The FET switch of Claim 2 wherein the resistor has a value of substantially 10K ohms.

11. In an ABS braking system, an FET switch for PWM the current through a control solenoid comprising:

an FET switching transistor having a conductive path coupled to the solenoid at a node;

a reverse voltage breakdown diode and a series resistor being coupled between the node and a gate of the FET switching transistor;

a detector responsive to current flow through the reverse breakdown diode to generate a surge control signal;

a first biasing current source coupled to the gate, the first biasing current source enabling the FET switching transistor to be turned off fast enough to generate a voltage surge at the node caused by the inductance of the control solenoid, which would exceed the BVdss of the FET switching transistor;

a second biasing current source coupled to the gate, the second current source biasing current; and

a biasing current switching circuit coupled to the first biasing circuit to disconnect flow of first biasing current in response to the surge control signal.

12. The FET switch of Claim 11 wherein the reverse breakdown diode is a zener diode.

13. The FET switch of Claim 11 wherein the current flow through the reverse breakdown diode is sufficient to overcome the second current source biasing current to turn on the FET switching transistor to clamp the voltage surge at a voltage below the BVdss of the FET switching transistor.

14. The FET switch of Claim 11 wherein the first bias current is substantially 20 ma. and the second bias current is substantially 80 microamps.

15. The FET switch of Claim 11 wherein the resistor has a value of substantially 10K ohms.

16. The FET switch of Claim 11 wherein the FET switching transistor is a power FET having load current of substantially 5A.

17. The FET switch of Claim 11 wherein the FET switching transistor, the reverse breakdown diode, resistor, first and second biasing current sources, the detector and the biasing current switching circuit are all integrated onto an integrated circuit.

18. The FET switch of Claim 17 wherein a plurality of FET switches are integrated onto a single integrated circuit.

19. A clamp circuit comprising:

a reverse breakdown diode and a resistor coupled in series thereto coupled between a load and a gate of an FET transistor;

a surge detector coupled to the reverse breakdown diode and responsive to current flow therein;

a first switchable current source coupled to the gate providing a first biasing current and responsive to an output signal from the surge detector;

a second current source coupled to the gate providing a second biasing current less than the first biasing current, whereby the detection of a surge by the surge detector disconnects the first biasing current to allow the current flowing through the reverse breakdown diode to turn on the FET transistor to clamp the surge voltage below the BVdss thereof.

20. The clamp circuit of Claim 19 wherein the FET transistor is a power FET switching transistor and the load is an inductive load.